

## SYSTEM FOR IMPROVING PCI WRITE PERFORMANCE

### ABSTRACT

A method and apparatus for traversing a queue of commands containing a mixture of read and write commands places a Next Valid Write Address pointer in each queue entry. In this manner, time savings are achieved by allowing preprocessing of the next write command to be executed. The method may be practiced by setting a next valid address pointer in all queue entries. Queue traversal may be forward, backward, or bi-directional.